

## CLAIMS

1. A method of encrypting a digital signal comprising:  
2 generating a plurality of pseudo-noise sequences;  
4 combining said pseudo-noise sequences, or portions thereof, to generate  
an augmented pseudo-noise sequence; and  
encrypting a data stream using the augmented pseudo-noise sequence.
2. The method of claim 1 wherein said generating step comprises the  
2 step of generating first and second pseudo-noise sequences.
3. The method of claim 1 wherein said generating step comprises the  
2 step of generating three or more pseudo-noise sequences.
4. The method of claim 1 wherein said combining step comprises the  
2 step of inserting a segment of a first pseudo-noise sequence into a second  
pseudo-noise sequence at an arbitrary position in said second pseudo-noise  
4 sequence.
5. The method of claim 4 wherein said segment has an arbitrary  
2 length.
6. The method of claim 4 wherein said segment has arbitrary starting  
2 and ending positions within said first pseudo-noise sequence.
7. The method of claim 1 and further comprising the step of starting  
2 the output of the augmented pseudo-noise sequence at an arbitrary position in  
the sequence.
8. The method of claim 1 and further comprising the step of  
2 synchronizing the augmented pseudo-noise sequence to a reference clock.

9. The method of claim 8 wherein said synchronizing step comprises  
2 the step of synchronizing the augmented pseudo-noise sequence to a reference  
clock relative to an arbitrary offset.

*Sub*  
*AB*  
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10. Apparatus for encrypting a digital signal comprising:  
two or more pseudo-noise sequence generators  
circuitry for combining said pseudo-noise sequences, or portions thereof,  
4 to generate an augmented pseudo-noise sequence; and  
an encrypting circuit for correlating the augmented pseudo-noise  
6 sequence with a data stream.

*B1*  
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11. The apparatus of claim 10 wherein said generating step comprises  
the step of generating first and second pseudo-noise sequences.

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12. The apparatus of claim 10 wherein said two or more pseudo-noise  
sequence generators comprises three or more pseudo-noise sequence generators.

*Sub*  
*AB*  
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13. The apparatus of claim 10 wherein said combining circuitry  
comprises circuitry for inserting a segment of a first pseudo-noise sequence into  
a second pseudo-noise sequence at an arbitrary position in said second pseudo-  
4 noise sequence.

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14. The apparatus of claim 13 wherein said segment has an arbitrary  
length.

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15. The apparatus of claim 13 wherein said segment has arbitrary  
starting and ending positions within said first pseudo-noise sequence.

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16. The apparatus of claim 13 wherein said encrypting circuit performs  
an exclusive-or operation.

17. The apparatus of claim 10 and further comprising circuitry for  
2 starting the output of the augmented pseudo-noise sequence at an arbitrary  
position in the sequence.

18. The apparatus of claim 10 and further comprising circuitry for  
2 synchronizing the augmented pseudo-noise sequence to a reference clock.

19. The apparatus of claim 18 wherein said synchronizing circuitry  
2 comprises circuitry for synchronizing the augmented pseudo-noise sequence to a  
reference clock relative to an arbitrary offset.